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| Application No. 09 607 625 | Prepared by | LH | Tracking Number |
| Examiner-GAU Nguyen 2811 | Date | 5-17-04 | ~~Week Date~~ |
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| JACKET | | | |
|---|---|---|---|
| a. Serial No. | f. Foreign Priority | k. Print Claim(s) | p. PTO-1449 |
| b. Applicant(s) | g. Disclaimer | l. Print Fig. | q. PTOL-85b |
| c. Continuing Data | h. Microfiche Appendix | m. Searched Column | r. Abstract |
| d. PCT | i. Title | n. PTO-270/328 | (s) ~~Sheets/Figs~~ |
| e. Domestic Priority | j. Claims Allowed | o. PTO-892 | t. Other |

**SPECIFICATION**

a. Page Missing
b. Text Continuity
c. Holes through Data
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f. Duplicate Text
(g) Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

**CLAIMS**

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
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j. Duplicate Text
k. Other

**MESSAGE** i) Brief descript: The brief descript p. 22 lines 20-22 Fig 6 refers back to Fig 6.

Please resolve

Thanks

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**RESPONSE**

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1. Figure 1 is a cross-sectional view of a prior art semiconductor device shown at a fabrication stage whereby anti-reflective coating portions overlying various memory element regions will be subjected to various etching process steps after patterning.
2. Figure 2 is a cross-sectional view of a semiconductor substrate shown at a fabrication stage in accordance with the present invention where a first anti-reflective coating has been utilized for patterning core and periphery substrate regions.
3. Figure 3 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 2 shown with the first coat of anti-reflective coating having been removed.
4. Figure 4 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 3 shown at a fabrication stage where a second anti-reflective coating has been formed over the patterned core and peripheral regions in accordance with the present invention.
5. Figure 5 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 4 shown having patterned peripheral memory regions and core memory regions fully coated with the second anti-reflective coating.
6. Figure 6 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 6 shown having sidewall spacers formed from the second anti-reflective coating in accordance with the present invention.

Please Note

## DETAILED DESCRIPTION OF THE INVENTION

**[0006]** Figure 1 is a cross-section of a prior art semiconductor substrate 10 shown at an early fabrication stage for forming a flash memory device 100. As depicted, substrate 10 comprises a core region 10C and a periphery region 10P. The core memory stacks 12, 13 and periphery memory region 9 are provided with an anti-reflective coating 14 having a typical thickness d in a range of 300 Å to 1000 Å. Core memory stacks 12, 13, at this stage of fabrication and as depicted in Figure 1, may comprise a thin layer of silicon dioxide 11, a first polysilicon layer P1, a dielectric layer D1 over layer P1 and a second polysilicon layer P2 over layer D1. The spacing S between stacks 12 and 13 is in the sub-micron range which necessitates the formation of spacers between stacks 12 and 13 to protect the corner regions 11a of the silicon dioxide layers 11 during various etching operations. The peripheral memory region 9 may comprise, as depicted in Figure 1, a layer of polysilicon material P2 for use in formation of the periphery